PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-031816

(43)Date of publication of application : 02.02.1999

(51)Int.Cl. H01L 29/78
H01L 21/8238
H01L 27/092

(21)Application number : 09-188058

(22)Date of filing : 14.07.1997

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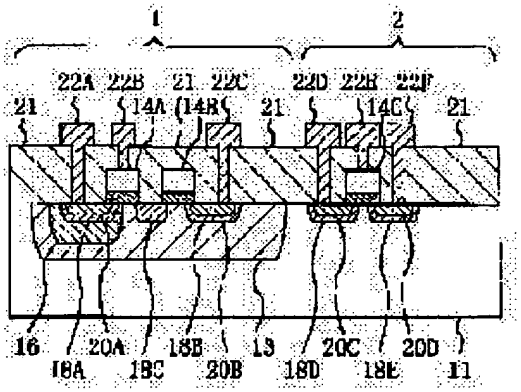
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To decrease variations in on the resistances of DMOSFETs in a semiconductor device having DMOSFETs.

SOLUTION: A DMOSFET 1 and a MOSFET 2 are formed on a semiconductor substrate 11 of P-type silicon. A first insulating gate electrode 14A and a dummy second insulating gate electrode 14B as a member for controlling the position of a drain contact region are formed at an established interval on an N-type drain region 13 of the DMOSFET 1. In the drain region 13, a P-type body region 16 is formed in self-alignment with respect to the first insulating gate electrode 14A in the region opposing second insulating region, and an N-type drain contact region 20B is formed in self-alignment with the second insulating gate electrode 14B in the region opposing first insulating region.



LEGAL STATUS

[Date of request for examination] 05.12.2000

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to DMOSFET which controls a high current, and its manufacture method about a semiconductor device and its manufacture method.
[0002]
[Description of the Prior Art] In recent years, many proposals about the semiconductor accumulation equipment by which DMOSFET (Double Diffused MOSFET) which is the device for a drive of various devices was integrated with other devices are made.
[0003] It explains referring to a drawing about the conventional manufacture method of DMOSFET currently indicated by JP,3-205832,A etc. hereafter.
[0004] Drawing 10 (a) - (c) forms in the principal plane of the n type semiconductor substrate 100 used as a drain field first the insulated-gate electrode 101 which consists of polycrystal silicon etc., as the cross-section composition of the order of a process of the manufacture method of the conventional DMOSFET is shown and it is shown in drawing 10 (a). Next, as shown in drawing 10 (b), the body field 102 of P type is formed in one [to the insulated-gate electrode 101 in the upper part of the semiconductor substrate 100] field of the direction of gate length by doping the impurity of P type by using the insulated-gate electrode 101 as a mask. Then, as shown in drawing 10 (c), while forming the source field 103 for the insulated-gate electrode 101 as some masks to the body field 102 of the semiconductor substrate 100 Using a photolithography to the body field 102 in the semiconductor substrate 100, and the field of an opposite side After forming the resist pattern (not shown) which has predetermined length from the edge by the side of the anti-body field of the insulated-gate electrode 101, the drain contact field 104 is formed by using this resist pattern as a mask. Then, an element will be completed if an electrode is formed in the source field 103 and the drain contact field 104, respectively.
[0005] Thus, DMOSFET has the effect that the efficiency-channel length of the channel field this body field 102 comes to be reversed of a field can be optimized independently of the gate length of the insulated-gate electrode 101, in the field of the insulated-gate electrode 101 bottom in the body field 102 while aiming at improvement in pressure-proofing of an element by preparing a predetermined interval between the insulated-gate electrode 101 and the drain contact field 104.
[0006]
[Problem(s) to be Solved by the Invention] However, the manufacture method of the semiconductor device containing the aforementioned conventional DMOSFET has the problem that dispersion in an on resistance arises. That is, the on resistance which is resistance between source drain contacts at the time of the flow of DMOSFET is greatly dependent on the distance between the insulated-gate electrode 101 and the drain contact field 104. Since this distance is determined by the alignment of a photolithography process, it will need to expect a margin in the size of a mask pattern at this alignment, therefore dispersion will produce it inevitably.
[0007] this invention solves the aforementioned conventional problem and aims at decreasing dispersion

in an on resistance in the semiconductor device which has DMOSFET, and its manufacture method.
[0008]
[Means for Solving the Problem] In order to attain the aforementioned purpose, on a semiconductor substrate, this invention sets an insulated-gate electrode and an interval, and is formed, and the drain contact region specification-part material which regulates the position of a drain contact field on a self-adjustment target is prepared.
[0009] The drain field where the semiconductor device concerning this invention is formed in a semiconductor substrate, and it comes to dope the low concentration impurity of the 1st conductivity type, The insulated-gate electrode which was insulated with the semiconductor substrate and formed on the drain field, The drain contact region specification-part material which the portion which sets an insulated-gate electrode and an interval, is formed on a drain field, and touches a semiconductor substrate at least becomes from an insulator, The body field where it is formed in the field of the opposite side of the drain contact region specification-part material to the insulated-gate electrode in a drain field, and comes to dope the impurity of the 2nd conductivity type, The source field where the periphery and interval of this body field are set to a body field, and it is formed in it, and comes to dope the high concentration impurity of the 1st conductivity type, It is formed in the field of the opposite side of an insulated-gate electrode to the drain contact region specification-part material in a drain field. It has the drain contact field where it comes to dope the high concentration impurity of the 1st conductivity type, and the position of the edge by the side of the source field in a drain contact field is regulated by the self-adjustment target according to the side by the side of the anti-source field of drain contact region specification-part material.
[0010] According to the semiconductor device of this invention, set an interval to the drain field on a semiconductor substrate mutually with an insulated-gate electrode, and it is formed in it. Have the drain contact region specification-part material which the portion which touches a semiconductor substrate at least becomes from an insulator, and the position of the edge by the side of the source field in a drain contact field Since it is regulated by the self-adjustment target according to the side by the side of the anti-source field of drain contact region specification-part material, dispersion in the distance during source drain contact can be suppressed.
[0011] As for the semiconductor device of this invention, it is desirable that it was formed in the field between the insulated-gate electrodes and drain contact region specification-part material in a semiconductor substrate, and the impurity of the 1st conductivity type is further equipped with the low resistance field which it comes to dope smaller [the high impurity concentration is larger than a drain field, and] than a source field or a drain contact field.
[0012] In the semiconductor device of this invention, an insulated-gate electrode is the 1st insulated-gate electrode, and, as for drain contact region specification-part material, it is desirable that it is the 2nd insulated-gate electrode which was insulated with the semiconductor substrate and formed.
[0013] As for the 1st insulated-gate electrode and the 2nd insulated-gate electrode, in the semiconductor device of this invention, connecting electrically is desirable.
[0014] The semiconductor device of this invention sets an interval to the field between the insulated-gate electrodes and drain contact region specification-part material on a semiconductor substrate with an insulated-gate electrode and a drain contact field, respectively, and is formed in it. The source drain extension member which the portion which touches a semiconductor substrate at least becomes from an insulator, It is formed in the field between the insulated-gate electrode in a semiconductor substrate, and a source drain extension member, and the field between a source drain extension member and drain contact region specification-part material, respectively. It is desirable that the impurity of the 1st conductivity type is further equipped with the low resistance field which it comes to dope smaller [the high impurity concentration is larger than a drain field, and] than a source field or a drain contact field.
[0015] In the semiconductor device of this invention, an insulated-gate electrode is the 1st insulated-gate electrode, it is the 2nd insulated-gate electrode which drain contact region specification-part material was insulated with the semiconductor substrate, and was formed, and, as for a source drain extension member, it is desirable that it is the 3rd insulated-gate electrode which was insulated with the

semiconductor substrate and formed.
[0016] As for the 1st insulated-gate electrode, the 2nd insulated-gate electrode, and the 3rd insulated-gate electrode, in the semiconductor device of this invention, connecting electrically is desirable.
[0017] The source side impurity diffusion field which the semiconductor device of this invention is formed in the field between the soffit section sides of a source field the upper-limit section side of the body field in a semiconductor substrate, and has the same high-impurity-concentration profile as a low resistance field, It is desirable for it to have been formed in the field between the soffit section sides of the drain field in a semiconductor substrate and a drain contact field, and to have further the low resistance field and the drain contact side impurity diffusion field which has the same high-impurity-concentration profile.
[0018] In the semiconductor device of this invention in the both-sides side of the direction of gate length of an insulated-gate electrode and drain contact region specification-part material The side attachment wall which consists of an insulator layer, respectively sticks, is formed, and the position of the edge by the side of the drain contact field in a source field While being regulated by the self-adjustment target by the side attachment wall by the side of the anti-drain contact field of an insulated-gate electrode, the position of the edge by the side of the source field in a drain contact field It is desirable to be regulated by the self-adjustment target by the side attachment wall by the side of the anti-source field of drain contact region specification-part material.
[0019] The manufacture method of the 1st semiconductor device concerning this invention The drain field formation process which forms a drain field by doping the impurity of the 1st conductivity type to a semiconductor substrate at low concentration, The insulated-gate electrode formation process which sets and forms for an interval the 1st insulated-gate electrode and 2nd insulated-gate electrode of each other which are insulated with this drain field, respectively on a drain field, the 1st insulated-gate electrode [in / a drain field / using the 1st insulated-gate electrode as a mask] -- anti- -- by doping the impurity of the 2nd conductivity type to the 1st field by the side of the 2nd insulated-gate electrode The body field formation process which forms a body field in the 1st field at a self-adjustment target, and by doping the impurity of the 1st conductivity type to a body field by using the 1st insulated-gate electrode as a mask at high concentration A source field on a self-adjustment target to a body field And the source field formation process formed so that the periphery and interval of a body field may be set, the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode as a mask] -- anti- -- by doping the impurity of the 1st conductivity type at high concentration to the 2nd field by the side of the 1st insulated-gate electrode It has the drain contact field formation process which forms a drain contact field in the 2nd field at a self-adjustment target.
[0020] The insulated-gate electrode formation process which sets and forms for an interval the 1st insulated-gate electrode and 2nd insulated-gate electrode of each other which are insulated with this drain field, respectively on a drain field according to the manufacture method of the 1st semiconductor device, the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode as a mask] -- anti- -- by doping the impurity of the 1st conductivity type to the field by the side of the 1st insulated-gate electrode at high concentration Since it has the drain contact field formation process which forms a drain contact field in a self-adjustment target, the position of the edge by the side of the source field in a drain contact field Since it is regulated by the side by the side of the anti-source field of the 2nd insulated-gate electrode, dispersion in the distance during source drain contact can be suppressed.
[0021] The manufacture method of the 2nd semiconductor device concerning this invention The drain field formation process which forms a drain field by doping the impurity of the 1st conductivity type to a semiconductor substrate at low concentration, The insulated-gate electrode formation process which sets and forms for an interval the 1st insulated-gate electrode and 2nd insulated-gate electrode of each other which are insulated with this drain field, respectively on a drain field, After depositing an insulator layer over the whole surface on a semiconductor substrate, while forming in the both-sides side by the side of the direction of gate length of the 1st insulated-gate electrode the 1st side attachment wall which consists of an insulator layer by performing etchback to this insulator layer The side-attachment-wall

formation process which forms in the both-sides side by the side of the direction of gate length of the 2nd insulated-gate electrode the 2nd side attachment wall which consists of an insulator layer, the 1st insulated-gate electrode [in / a drain field / using the 1st insulated-gate electrode and the 1st side attachment wall as a mask] -- anti- -- by doping the impurity of the 2nd conductivity type to the 1st field by the side of the 2nd insulated-gate electrode The body field formation process which forms a body field in the 1st field at a self-adjustment target, and by doping the impurity of the 1st conductivity type to a body field at high concentration by using the 1st insulated-gate electrode and the 1st side attachment wall as a mask A source field on a self-adjustment target to a body field And the source field formation process formed so that the periphery and interval of a body field may be set, the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode and the 2nd side attachment wall as a mask] -- anti- -- by doping the impurity of the 1st conductivity type at high concentration to the 2nd field by the side of the 1st insulated-gate electrode It has the drain contact field formation process which forms a drain contact field in the 2nd field at a self-adjustment target.

[0022] The insulated-gate electrode formation process which sets and forms for an interval the 1st insulated-gate electrode and 2nd insulated-gate electrode of each other which are insulated with this drain field, respectively on a drain field according to the manufacture method of the 2nd semiconductor device, The side-attachment-wall formation process which forms the 1st and 2nd side attachment walls which become each side by the side of the direction of gate length of the 1st and 2nd insulated-gate electrodes from an insulator layer, respectively, the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode and the 2nd side attachment wall as a mask] -- anti- -- by doping the impurity of the 1st conductivity type to the field by the side of the 1st insulated-gate electrode at high concentration Since it has the drain contact field formation process which forms a drain contact field in a self-adjustment target, the position of the edge by the side of the source field in a drain contact field Since it is regulated by the 2nd side attachment wall by the side of the anti-source field of the 2nd insulated-gate electrode, dispersion in the distance during source drain contact can be suppressed.

[0023] As for the manufacture method of the 1st or 2nd semiconductor device, it is desirable to equip further the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode in a semiconductor substrate with the impurity diffusion field formation process which forms an impurity diffusion field in the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode when high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field.

[0024] In the manufacture method of the 1st or 2nd semiconductor device an impurity diffusion field formation process The field between the upper-limit sections of a body field and the soffit sections of a source field in a semiconductor substrate, When high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field to the field between the soffit sections of a drain field and a drain contact field It is desirable to include the process which forms an impurity diffusion field in each field between the upper-limit section of a body field and the soffit section of a source field and between the soffit sections of a drain field and a drain contact field, respectively.

[0025] The manufacture method of the 3rd semiconductor device concerning this invention By doping the impurity of the 1st conductivity type to the semiconductor substrate of 1 at low concentration The drain field formation process which forms the drain field for DMOSFET, While setting and forming an interval mutually, the 1st insulated-gate electrode for DMOSFET and the 2nd insulated-gate electrode which are insulated with this drain field on a drain field, respectively The insulated-gate electrode formation process which forms the 3rd insulated-gate electrode for MOSFET which sets a drain field and an interval on the semiconductor substrate of 1, and is insulated with a semiconductor substrate, the 1st insulated-gate electrode [in / a drain field / using the 1st insulated-gate electrode as a mask] -- anti- -- by doping the impurity of the 2nd conductivity type to the 1st field by the side of the 2nd insulated-gate electrode The body field formation process which forms a body field in the 2nd field at a self-adjustment target, and by doping the impurity of the 1st conductivity type to a body field by using the 1st insulated-gate electrode as a mask at high concentration A source field on a self-adjustment target to

a body field And the source field formation process formed so that the periphery and interval of a body field may be set, the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode as a mask] -- anti- -- by doping the impurity of the 1st conductivity type at high concentration to the 2nd field by the side of the 1st insulated-gate electrode The drain contact field formation process which forms a drain contact field in the 2nd field at a self-adjustment target, By doping the impurity of the 1st conductivity type by using the 3rd insulated-gate electrode as a mask at high concentration to the 3rd field by the side of the 2nd [of the 3rd insulated-gate electrode in the semiconductor substrate of 1] insulated-gate electrode the 1st source drain field -- the 3rd field -- self, while forming so that a drain field and an interval may be set conformably the 3rd insulated-gate electrode in the semiconductor substrate of 1 -- anti- -- doping the impurity of the 1st conductivity type at high concentration to the 4th field by the side of the 2nd insulated-gate electrode -- the 2nd source drain field -- the 4th field -- self -- it has the source drain field formation process formed conformably

[0026] According to the manufacture method of the 3rd semiconductor device, while setting and forming an interval mutually, the 1st insulated-gate electrode for DMOSFET and the 2nd insulated-gate electrode which are insulated with this drain field on a drain field, respectively The insulated-gate electrode formation process which forms the 3rd insulated-gate electrode for MOSFET which sets a drain field and an interval on the semiconductor substrate of 1, and is insulated with a semiconductor substrate, the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode as a mask] -- anti- -- by doping the impurity of the 1st conductivity type to the field by the side of the 1st insulated-gate electrode at high concentration Since it has the drain contact field formation process which forms a drain contact field in a self-adjustment target, Since the position of the edge by the side of the source field in the drain contact field for DMOSFET is regulated by the side by the side of the anti-source field of the 2nd insulated-gate electrode, it can suppress dispersion in the distance during source drain contact.

[0027] Furthermore, without increasing the cost which manufacture of a semiconductor device takes, in order to form the 1st insulated-gate electrode for DMOSFET, the 2nd insulated-gate electrode, and the 3rd insulated-gate electrode for MOSFET at the process of 1, in case DMOSFET and MOSFET are formed on the semiconductor substrate of 1, DMOSFET to which dispersion in an on resistance decreased can be manufactured, and the 2nd insulated-gate electrode does not affect the electrical property of MOSFET.

[0028] The manufacture method of the 4th semiconductor device concerning this invention By doping the impurity of the 1st conductivity type to the semiconductor substrate of 1 at low concentration The drain field formation process which forms the drain field for DMOSFET, While setting and forming an interval mutually, the 1st insulated-gate electrode for DMOSFET and the 2nd insulated-gate electrode which are insulated with this drain field on a drain field, respectively The insulated-gate electrode formation process which forms the 3rd insulated-gate electrode for MOSFET which sets a drain field and an interval on the semiconductor substrate of 1, and is insulated with a semiconductor substrate, After depositing an insulator layer over the whole surface on the semiconductor substrate of 1, by performing etchback to this insulator layer The 1st side attachment wall which consists of an insulator layer is formed in the both-sides side by the side of the direction of gate length of the 1st insulated-gate electrode. The side-attachment-wall formation process which forms in the both-sides side by the side of the direction of gate length of the 2nd insulated-gate electrode the 2nd side attachment wall which consists of an insulator layer, and forms in the both-sides side by the side of the direction of gate length of the 3rd insulated-gate electrode the 3rd side attachment wall which consists of an insulator layer, the 1st insulated-gate electrode [in / a drain field / using the 1st insulated-gate electrode and the 1st side attachment wall as a mask] -- anti- -- by doping the impurity of the 2nd conductivity type to the 1st field by the side of the 2nd insulated-gate electrode The body field formation process which forms a body field in the 1st field at a self-adjustment target, and by doping the impurity of the 1st conductivity type to a body field at high concentration by using the 1st insulated-gate electrode and the 1st side attachment wall as a mask A source field on a self-adjustment target to a body field And the source field formation process formed so that the periphery and interval of a body field may be set, the 2nd insulated-gate

electrode [in / a drain field / using the 2nd insulated-gate electrode and the 2nd side attachment wall as a mask] -- anti- -- by doping the impurity of the 1st conductivity type at high concentration to the 2nd field by the side of the 1st insulated-gate electrode The drain contact field formation process which forms a drain contact field in the 2nd field at a self-adjustment target, By doping the impurity of the 1st conductivity type by using the 3rd insulated-gate electrode as a mask at high concentration to the 3rd field by the side of the 2nd [of the 3rd insulated-gate electrode in the semiconductor substrate of 1] insulated-gate electrode the 1st source drain field -- the 3rd field -- self, while forming so that a drain field and an interval may be set conformably the 3rd insulated-gate electrode in the semiconductor substrate of 1 -- anti- -- doping the impurity of the 1st conductivity type at high concentration to the 4th field by the side of the 2nd insulated-gate electrode -- the 2nd source drain field -- the 4th field -- self -- it has the source drain field formation process formed conformably

[0029] According to the manufacture method of the 4th semiconductor device, while setting and forming an interval mutually, the 1st insulated-gate electrode for DMOSFET and the 2nd insulated-gate electrode which are insulated with this drain field on a drain field, respectively The insulated-gate electrode formation process which forms the 3rd insulated-gate electrode for MOSFET which sets a drain field and an interval on the semiconductor substrate of 1, and is insulated with a semiconductor substrate, the 1- with the side-attachment-wall formation process which forms the 1st - the 3rd side attachment wall which become each side by the side of the direction of gate length of the 3rd insulated-gate electrode from an insulator layer, respectively the 2nd insulated-gate electrode [in / a drain field / using the 2nd insulated-gate electrode and the 2nd side attachment wall as a mask] -- anti- -- by doping the impurity of the 1st conductivity type to the field by the side of the 1st insulated-gate electrode at high concentration Since it has the drain contact field formation process which forms a drain contact field in a self-adjustment target, Since the position of the edge by the side of the source field in the drain contact field for DMOSFET is regulated by the side by the side of the anti-source field of the 2nd insulated-gate electrode, dispersion in the distance during source drain contact can be suppressed.

[0030] Furthermore, without increasing the cost which manufacture of a semiconductor device takes, in order to form the 1st insulated-gate electrode for DMOSFET, the 2nd insulated-gate electrode, and the 3rd insulated-gate electrode for MOSFET at the process of 1, in case DMOSFET and MOSFET are formed on the semiconductor substrate of 1, DMOSFET to which dispersion in an on resistance decreased can be manufactured, and the 2nd insulated-gate electrode does not affect the electrical property of MOSFET.

[0031] The manufacture method of the 3rd or 4th semiconductor device to the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode in the semiconductor substrate of 1 When high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field It is desirable to have further the impurity diffusion field formation process which forms an impurity diffusion field in the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode.

[0032] In the manufacture method of the 3rd or 4th semiconductor device an impurity diffusion field formation process The field between the upper-limit sections of a body field and the soffit sections of a source field in the semiconductor substrate of 1, When high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field to the field between the soffit sections of a drain field and a drain contact field The process which forms an impurity diffusion field in each field between the upper-limit section of a body field, and the soffit section of a source field, and between the soffit sections of a drain field and a drain contact field, respectively, To the field by the side of the soffit section of the 1st source drain field in the semiconductor substrate of 1, and the field by the side of the soffit section of the 2nd source drain field When high impurity concentration dopes the impurity of the 1st conductivity type smaller than the 1st and 2nd source drain fields It is desirable to include the process which forms an impurity diffusion field in the field by the side of the soffit section of the 1st source drain field and the field by the side of the soffit section of the 2nd source drain field, respectively.

[0033] As for the manufacture method of the 1st - the 4th semiconductor device, it is desirable to have

further the process which connects electrically the 1st insulated-gate electrode and the 2nd insulated-gate electrode.
[0034]
[Embodiments of the Invention]
(1st operation gestalt) It explains, referring to a drawing about the 1st operation gestalt of this invention.
[0035] Drawing 1 shows the cross-section composition of the semiconductor device concerning the 1st operation gestalt of this invention. drawing 1 -- setting -- the conductivity type of an impurity -- P type -- and DMOSFET1 and MOSFET2 set a predetermined interval to the semiconductor substrate 11 which a field direction becomes from the silicon single crystal of (100), and they are formed in it In DMOSFET1, on the principal plane of the semiconductor substrate 11, the drain field 13 of N type is formed, and a gate insulator layer intervenes between the upper surfaces of the drain field 13, respectively, and 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B as drain contact region specification-part material set an interval mutually, and are formed at the upper part of the semiconductor substrate 11. The body field 16 of P type is formed in the field of an opposite side to 1st insulated-gate electrode 14A at the self-adjustment target to 2nd insulated-gate electrode 14B of 1st insulated-gate electrode 14A in the upper part of the drain field 13, and this body field 16 is equivalent to the P type substrate in the case of N channel MOSFET. Conformably, the periphery and interval of the body field 16 are set and it is formed. source side impurity diffusion field 18A of the low concentration [upper part / of the body field 16] of N type with larger high impurity concentration than the drain field 13 -- 1st insulated-gate electrode 14A -- receiving -- self -- As opposed to 1st insulated-gate electrode 14A of 2nd insulated-gate electrode 14B in the upper part of the drain field 13 in the field of an opposite side Low-concentration drain contact side impurity diffusion field 18B of N type with larger high impurity concentration than the drain field 13 is formed in the self-adjustment target to 2nd insulated-gate electrode 14B. Low resistance field 18C of the N type which is the same high impurity concentration as source side impurity diffusion field 18A and drain contact side impurity diffusion field 18B is formed in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the upper part of the drain field 13. Conformably, the periphery and interval of source side impurity diffusion field 18A are set, and it is formed. source field 20A of high concentration [upper part / of source side impurity diffusion field 18A / A / source side impurity diffusion field 18] -- 1st insulated-gate electrode 14A -- receiving -- self -- In the upper part of drain contact side impurity diffusion field 18B drain contact field 20B of high concentration [B / drain contact side impurity diffusion field 18] -- 2nd insulated-gate electrode 14B -- receiving -- self -- conformably, the periphery and interval of drain contact side impurity diffusion field 18B are set, and it is formed On the semiconductor substrate 11, the NSG film 21 as a layer insulation film accumulates, and drain wiring 22C for connecting with 1st gate wiring 22B for connecting with source wiring 22A for connecting with source field 20A electrically and 1st insulated-gate electrode 14A electrically and drain contact field 20B electrically is formed at this NSG film 21, respectively.
[0036] In MOSFET2, the drain field 13 of DMOSFET1 and a predetermined interval are set to the principal plane of the semiconductor substrate 11, and 3rd insulated-gate electrode 14C is formed in it. In the field by the side of 2nd [of 3rd insulated-gate electrode 14C in the upper part of the semiconductor substrate 11] insulated-gate electrode 14B Conformable drain field 13 of DMOSFET1 and predetermined interval are set, and it is formed. 1st low concentration diffusion field 18D of N type with larger high impurity concentration than the drain field 13 -- 3rd insulated-gate electrode 14C -- receiving -- self -- 3rd insulated-gate electrode 14C in the upper part of the semiconductor substrate 11 -- anti- -- the field by the side of 2nd insulated-gate electrode 14B -- 2nd low concentration diffusion field 18E of N type with larger high impurity concentration than the drain field 13 -- 3rd insulated-gate electrode 14C -- receiving -- self -- it is formed conformably Conformably, the 1st periphery and interval of low concentration diffusion field 18D are set, and it is formed. 1st source drain field 20C of high high impurity concentration [upper part / of 1st low concentration diffusion field 18D] -- 3rd insulated-gate electrode 14C -- receiving -- self -- 2nd source drain field 20D of high concentration [upper part / of 2nd low concentration diffusion field 18E] -- 3rd insulated-gate electrode 14C --

h g cg b eb cg e e

receiving -- self -- conformably, the 2nd periphery and interval of low concentration diffusion field 18E are set, and it is formed The 2nd source drain wiring 22F for connecting with 2nd gate wiring 22E for connecting with 1st source drain wiring 22D for connecting with 1st source drain field 20C electrically and 3rd insulated-gate electrode 14C electrically and 2nd source drain field 20D electrically is formed in the NSG film 21, respectively.

[0037] Thus, according to this operation gestalt, in DMOSFET1, it has the same composition as the 1st insulated-gate electrode. Since 2nd insulated-gate electrode 14B which is a dummy is formed in the field between 1st insulated-gate electrode 14A and drain contact field 20B in a principal plane at the semiconductor substrate 11, Since the distance of source field 20A and drain contact field 20B is regulated by the position of the edge by the side of drain contact field 20B of 2nd insulated-gate electrode 14B at a self-adjustment target Dispersion in the distance during the source drain contact which determines an on resistance can be suppressed.

[0038] Furthermore, in this operation gestalt, since low resistance field 18C with the larger high impurity concentration of N type than a drain field is prepared in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the upper part of the semiconductor substrate 11, it is between the source drain contacts in the upper part of the semiconductor substrate 11 and resistance of these low resistance field 18 C parts becomes small, an on resistance decreases.

[0039] Moreover, each high concentration impurity range of source field 20A, drain contact field 20B, 1st source drain field 20C, and 2nd source drain field 20D Since it is surrounded by the low-concentration impurity ranges 18A, 18B, 18D, and 18E, respectively and has the so-called DOD structure, Though high electric field are impressed to each high concentration impurity range, since the electric field of the periphery of each high concentration impurity range are eased, pressure-proofing of both the equipments of DMOSFET1 and MOSFET2 improves further.

[0040] It explains referring to a drawing about the manufacture method of the semiconductor device concerning this operation gestalt hereafter.

[0041] Drawing 2 and drawing 3 show the cross-section composition of the order of a process in the manufacture method of the semiconductor device concerning this operation gestalt. As shown in drawing 2 (a), specific resistance the field (100) of a field direction by 10 - 20 ohm-cm first, on the semiconductor substrate 11 of the P type made into a principal plane The 1st resist pattern 12 is used as a mask. after forming in the drain formation field for DMOSFET1 the 1st resist pattern 12 which has opening -- this -- For example, the phosphorus ion as low-concentration N type impurity ion whose dose pouring energy is 100keV(s) and is about [2x1012cm -] two is injected into the semiconductor substrate 11. Then, the drain field 13 is formed by heat-treating to this semiconductor substrate 11, and activating phosphorus ion.

[0042] Next, as shown in drawing 2 (b), after performing thermal oxidation whose temperature is 900 degrees C and forming in the upper part of the semiconductor substrate 11 the gate oxide film 24 whose thickness is about 15nm as opposed to the semiconductor substrate 11, the polycrystal silicon film 25 is deposited over the whole surface on the semiconductor substrate 11. Then, it etches alternatively to the polycrystal silicon film 25, and an interval is mutually set to the drain field 13 on the semiconductor substrate 11, it becomes it from the gate oxide film 24 and the polycrystal silicon film 25, and 1st insulated-gate electrode 14A for DMOSFET1, 2nd insulated-gate electrode formation 14B of a dummy, and 3rd insulated-gate electrode 14C for MOSFET2 are formed in it.

[0043] Next, as shown in drawing 2 (c), after forming the 2nd resist pattern 15 which has opening to the body formation field for DMOSFET1 on the semiconductor substrate 11, The edge by the side of the 2nd insulated-gate electrode is used as a mask. this -- the 2nd resist pattern 15 and 1st insulated-gate electrode 14A -- anti- -- For example, the boron ion as P type impurity ion whose dose pouring energy is 140keV(s) and is about [1x1014cm -] two is poured into the drain field 13 of the semiconductor substrate 11. Then, the body field 16 is formed in a self-adjustment target to 1st insulated-gate electrode 14A by heat-treating to this semiconductor substrate 11, and activating boron ion.

[0044] Next, as shown in drawing 2 (d), after forming the 3rd resist pattern 17 which has opening, respectively to the N type low concentration impurity diffusion formation field for DMOSFET1, and the

N type low concentration diffusion formation field for MOSFET2 on the semiconductor substrate 11, The edge of each gate-length direction of the 3rd insulated-gate electrode 14A, 14B, and 14C is used as a mask. this -- the 3rd resist pattern 17 and the 1- For example, the phosphorus ion as low-concentration N type impurity ion whose dose pouring energy is 30keV(s) and is about [1x1013cm -] two is poured into the upper part of the semiconductor substrate 11. Then, by heat-treating to this semiconductor substrate 11, and activating phosphorus ion Source side impurity diffusion field 18A in DMOSFET1, drain contact side impurity diffusion field 18B, and low resistance field 18C, And 1st low concentration diffusion field 18D and 2nd low concentration diffusion field 18E in MOSFET2 are formed in a self-adjustment target to each insulated-gate electrodes 14A, 14B, and 14C, respectively.

[0045] As shown in drawing 3 (a), on the semiconductor substrate 11 Next, the source formation field and drain contact formation field for DMOSFET1, And after forming in the source drain formation field for MOSFET2 the 4th resist pattern 19 which has opening, respectively, Each edge of the direction of gate length of the 3rd insulated-gate electrode 14A, 14B, and 14C is used as a mask. this -- the 4th resist pattern 19 and the 1- For example, the arsenic ion as high-concentration N type impurity ion whose dose pouring energy is 30keV(s) and is about [1x1016cm -] two is poured into the upper part of the semiconductor substrate 11. Then, by heat-treating to this semiconductor substrate 11, and activating arsenic ion Source field 20A and drain contact field 20B in DMOSFET1, And 1st source drain field 20C and 2nd source drain field 20D in MOSFET2 are formed in a self-adjustment target to each insulated-gate electrodes 14A, 14B, and 14C, respectively.

[0046] Next, as shown in drawing 3 (b), thickness deposits over the whole surface on the semiconductor substrate 11 using reduced pressure CVD by using as a layer insulation film the NSG film 21 which is about 800nm. Then, source field 20A [in / DMOSFET1 / to this NSG film 21 top], 1st insulated-gate electrode 14A, drain contact field 20B, and 1st source drain field 20C in MOSFET2, The resist pattern (not shown) which exposes a part of each upper surface of 3rd insulated-gate electrode 14C and 2nd source drain field 20D is formed. By performing dry etching to the NSG film 21 by using this resist pattern as a mask, a contact hole is formed, respectively. Then, after [for example,] depositing the metal membrane (not shown) which consists of aluminum etc. over the whole surface on the semiconductor substrate 11 using the sputtering method, By forming a predetermined resist pattern (not shown) on this metal membrane, and etching to this metal membrane by using this resist pattern as a mask 1st source drain wiring 22D in source wiring 22A in DMOSFET1, 1st gate wiring 22B, drain wiring 22C, and MOSFET2, 2nd gate wiring 22E, and the 2nd source drain wiring 22F are formed, respectively.

[0047] thus, 2nd insulated-gate electrode 14B of the dummy which is drain contact region specification-part material in the process which forms 1st insulated-gate electrode 14A of DMOSFET1 according to the manufacture method concerning this operation gestalt -- forming -- this -- 2nd insulated-gate electrode 14B -- anti- -- the edge by the side of the 1st insulated-gate electrode -- using -- drain contact field 20B -- self -- it forms conformably Since it becomes unnecessary to expect the margin of the size of the resist film at the time of resist film formation conventionally unlike the drain contact field using the resist film and is hard coming to generate dispersion in the distance during source drain contact by this consequently, dispersion in the on resistance in DMOSFET1 decreases. Since drain contact region specification-part material is considered as the same composition as 1st insulated-gate electrode 14A and it moreover is not necessary to establish a new process, most costs which form drain contact region specification-part material can be disregarded.

[0048] Furthermore, in the process which forms each low concentration diffusion fields 18D and 18E in MOSFET2, since low resistance field 18C with larger high impurity concentration than the drain field 13 is prepared in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the semiconductor substrate 11, the effect that the on resistance of DMOSFET1 decreases arises, without adding a new process. In addition, needless to say, 2nd insulated-gate electrode 14B and low resistance field 18C which are this drain contact region specification-part material do not affect a property at all to MOSFET2.

[0049] (The 1st modification of the 1st operation gestalt) It explains hereafter, referring to a drawing

about the 1st modification of this operation gestalt.
[0050] Drawing 4 shows the cross-section composition of the semiconductor device concerning the 1st modification of the 1st operation gestalt. In drawing 4 , explanation is omitted by giving the same sign to the same component as the component of drawing 1 . As shown in drawing 4 , it sets to DMOSFET1 as a feature of this modification. It is formed in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the principal plane of the semiconductor substrate 11. It has 4th insulated-gate electrode 14D as a source drain extension member which has the same composition as 2nd insulated-gate electrode 14B of a dummy. Furthermore, low resistance field 18F which have the high impurity concentration of the same N type as low resistance field 18C are formed in the field between 1st insulated-gate electrode 14A and 4th insulated-gate electrode 14D in the upper part of the semiconductor substrate 11.
[0051] Thus, according to this modification, improvement in pressure-proofing is aimed at by enlarging distance between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B.
[0052] Here, the case where enlarge distance between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B, and neither forms 4th insulated-gate electrode 14D as a source drain extension member and the low resistance fields 18C and 18F is considered. In this case, since the distance between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B becomes large, although pressure-proofing improves, the on resistance during source drain contact increases. Therefore, continuing and forming in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the upper part of the semiconductor substrate 11 the low resistance field where high impurity concentration is larger than the drain field 13 is also considered.
[0053] However, generally, in DMOSFET1, if voltage is impressed to drain contact field 20B An interface with the drain field 13 of the N type under 1st insulated-gate electrode 14A in the body field 16 of P type, Namely, since the depletion layer generated in the PN-junction side which consists of a body field 16 and a drain field 13 spreads in both directions of the direction of gate length, Source side impurity diffusion field 18A of N type is contacted, the so-called punch through occurs, and it becomes impossible to control a carrier by 1st insulated-gate electrode 14A. Here, in order to make a punch through hard to produce, it turns out that what is necessary is just to make small concentration by the side of drain contact field 20B of the body field 16 in the upper part of the semiconductor substrate 11 so that a depletion layer may spread in the drain contact field 20B side.
[0054] Therefore, in having formed the low resistance field which spreads succeeding the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the upper part of the semiconductor substrate 11 and where high impurity concentration is larger than the drain field 13 as mentioned above, since high impurity concentration by the side of drain contact field 20B cannot be made small, a punch through cannot be suppressed.
[0055] Then, in this modification, the low resistance fields 18C and 18F are formed in the field between the field between 1st insulated-gate electrode 14A and 4th insulated-gate electrode 14D in the upper part of the semiconductor substrate 11 and 2nd insulated-gate electrode 14B, and 4th insulated-gate electrode 14D, respectively. Since the drain field 13 where high impurity concentration is smaller than this low resistance field intervenes between each low resistance field, a depletion layer becomes easier to spread in the drain contact field 20B side. Consequently, it is hard coming to generate a punch through, and pressure-proofing can be raised.
[0056] On the contrary, since it becomes impossible to form a low resistance field when 2nd insulated-gate electrode 14B and 4th insulated-gate electrode 14D are formed in one, an on resistance will increase.
[0057] From the above thing, this modification between the source fields and drain contact fields in the principal plane of the semiconductor substrate 11 An interval is mutually set for a source drain extension member and drain contact position specification-part material. Coexistence with improvement in pressure-proofing and reduction of an on resistance is aimed at from preparing in the shape of a grid so to speak, and establishing the low resistance field where high impurity concentration is larger than the drain field 13 in the shape of a grid in the field between these members in the upper part of the

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semiconductor substrate 11.
[0058] In addition, in DMOSFET1 of drawing 4 , although the source drain extension member of one was prepared, you may prepare two or more source drain extension members in the range from which the relation between pressure-proofing and an on resistance becomes good.
[0059] (The 2nd modification of the 1st operation gestalt) It explains hereafter, referring to a drawing about the 2nd modification of this operation gestalt.
[0060] Drawing 5 shows the cross-section composition of the semiconductor device concerning the 2nd modification of the 1st operation gestalt. In drawing 5 , explanation is omitted by giving the same sign to the same component as the component of drawing 1 . As shown in drawing 5 , wiring with 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B is electrically connected as a feature of this modification using the 1st gate wiring 22G so that 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B can control to this potential.
[0061] If voltage is impressed to the 1st gate wiring, in order that a carrier may focus on the field of the 2nd insulated-gate electrode 14B bottom in the upper part of the semiconductor substrate 11 by this, an on resistance decreases further. Moreover, the property of MOSFET2 is not affected at all, without the cost which manufacture of DMOSFET1 takes increasing, since a new process is not needed.
[0062] In addition, even if it prepares 4th insulated-gate electrode 14D between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B and connects electrically 1st insulated-gate electrode 14A, 2nd insulated-gate electrode 14B, and 4th insulated-gate electrode 14D like the 1st aforementioned modification, it cannot be overemphasized that the same effect can be acquired.
[0063] (2nd operation gestalt) It explains, referring to a drawing about the 2nd operation gestalt of this invention.
[0064] Drawing 6 shows the cross-section composition of the semiconductor device concerning the 2nd operation gestalt of this invention. the component shown in drawing 1 in drawing 6 -- explanation is omitted by giving the same sign to the same component In the 1st operation gestalt, although each makes DOD structure the 1st of source field 20A of DMOSFET1, drain contact field 20B, and MOSFET2, and 2nd source drain fields 20C and 20D, the feature is that it makes each of each fields LDD structure in this operation gestalt. Therefore, in DMOSFET1, 1st sidewall 31A which is the 1st side attachment wall is formed in the both-sides side of the direction of gate length of 1st insulated-gate electrode 14A. 2nd sidewall 31B which is the 2nd side attachment wall is formed in the both-sides side of the direction of gate length of 2nd insulated-gate electrode 14B, and it sets to MOSFET2. 3rd sidewall 31C which is the 3rd side attachment wall is formed in the both-sides side of the direction of gate length of 3rd insulated-gate electrode 14C. It is the high-concentration source field of the N type formed conformably. DMOSFET1 -- setting -- 32A -- 1st insulated-gate electrode 14A -- anti- -- 1st sidewall 31A by the side of 2nd insulated-gate electrode 14B -- using -- self -- 32B -- 2nd insulated-gate electrode 14B -- anti- -- 2nd sidewall 31B by the side of 1st insulated-gate electrode 14A -- using -- self -- it is the high-concentration drain contact field of the N type formed conformably Similarly it is the 1st high-concentration source drain field of N type where 32C was formed in the self-adjustment target in MOSFET2 using 3rd sidewall 31C by the side of 2nd [of 3rd insulated-gate electrode 14C] insulated-gate electrode 14B. 32D -- 3rd insulated-gate electrode 14C -- anti- -- 3rd sidewall 31C by the side of the 2nd insulated-gate electrode -- using -- self -- it is the 2nd high-concentration source drain field of the N type formed conformably
[0065] Since each field is small only in the part in which the sidewall is formed, the low-concentration impurity diffusion fields 18A, 18B, 18D, and 18E are large conversely, respectively and the electric field of the periphery section of a high concentration impurity range are eased further, each of these high concentration impurity ranges of pressure-proofing improve further.
[0066] It explains referring to a drawing about the manufacture method of the semiconductor device concerning this operation gestalt hereafter.
[0067] Drawing 7 and drawing 8 show the cross-section composition of the order of a process in the manufacture method of the semiconductor device concerning this operation gestalt. As shown in drawing 7 (a), specific resistance the field (100) of a field direction by 10 - 20 ohm-cm first, on the

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semiconductor substrate 11 of the P type made into a principal plane The 1st resist pattern 12 is used as a mask. after forming in the drain formation field for DMOSFET1 the 1st resist pattern 12 which has opening -- this -- For example, the low-concentration phosphorus ion whose dose pouring energy is 100keV(s) and is about [2x1012cm -] two is injected into the semiconductor substrate 11, and the drain field 13 of N type is formed by heat-treating to this semiconductor substrate 11, and activating phosphorus ion after that.

[0068] Next, as shown in drawing 7 (b), after performing thermal oxidation whose temperature is 900 degrees C and forming in the upper part of the semiconductor substrate 11 the gate oxide film 24 whose thickness is about 15nm as opposed to the semiconductor substrate 11, the polycrystal silicon film 25 is deposited over the whole surface on the semiconductor substrate 11. Then, it etches alternatively to the polycrystal silicon film 25, the drain field 13 and interval on the semiconductor substrate 11 are set, it consists of a gate oxide film 24 and a polycrystal silicon film 25, and 1st insulated-gate electrode 14A for DMOSFET1, 2nd insulated-gate electrode formation 14B, and 3rd insulated-gate electrode 14C for MOSFET2 are formed.

[0069] Next, as shown in drawing 7 (c), after forming the 2nd resist pattern 15 which has opening to the body formation field for DMOSFET1 on the semiconductor substrate 11, The edge by the side of the 2nd insulated-gate electrode is used as a mask. this -- the 2nd resist pattern 15 and 1st insulated-gate electrode 14A -- anti- -- For example, the boron ion whose dose pouring energy is 140keV(s) and is about [1x1014cm -] two is poured into the drain field 13 of the semiconductor substrate 11. Then, the body field 16 of P type is formed in a self-adjustment target to 1st insulated-gate electrode 14A by heat-treating to this semiconductor substrate 11, and activating boron ion.

[0070] Next, as shown in drawing 7 (d), after forming the 3rd resist pattern 17 which has opening, respectively to the N type low concentration impurity diffusion formation field for DMOSFET1, and the low concentration diffusion formation field for MOSFET2 on the semiconductor substrate 11, The edge of each gate-length direction of the 3rd insulated-gate electrode 14A, 14B, and 14C is used as a mask. this -- the 3rd resist pattern 17 and the 1- For example, the low-concentration phosphorus ion whose dose pouring energy is 30keV(s) and is about [1x1013cm -] two is poured into the upper part of the semiconductor substrate 11. Then, by heat-treating to this semiconductor substrate 11, and activating phosphorus ion Source side impurity diffusion field 18A of the N type in DMOSFET1, drain contact side impurity diffusion field 18B of N type, and n type low resistance field 18C, And 1st low concentration diffusion field 18D of the N type in MOSFET2 and 2nd low concentration diffusion field 18E of N type are formed in a self-adjustment target to each insulated-gate electrodes 14A, 14B, and 14C, respectively.

[0071] Next, by crossing on the semiconductor substrate 11 on the whole surface, for example, depositing the silicon oxide (not shown) whose thickness is about 160nm, and performing isotropic etching to this silicon oxide after that, as shown in drawing 8 (a) 1st sidewall 31A is formed in the both-sides side by the side of the direction of gate length of 1st insulated-gate electrode 14A. 2nd sidewall 31B is formed in the both-sides side by the side of the direction of gate length of 2nd insulated-gate electrode 14B, and 3rd sidewall 31C is formed in the both-sides side by the side of the direction of gate length of 3rd insulated-gate electrode 14C. Here, as shown in drawing 8 (a), when the interval of 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B is narrow, 1st sidewall 31A and 2nd sidewall 31B which are formed between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B are formed in one.

[0072] As shown in drawing 8 (b), on the semiconductor substrate 11 Next, the source formation field and drain contact formation field for DMOSFET1, And after forming in the source drain formation field for MOSFET2 the 4th resist pattern 19 which has opening, respectively, Each sidewalls 31A, 31B, and 31C of the direction of gate length of the 3rd insulated-gate electrode 14A, 14B, and 14C are used as a mask. this -- the 4th resist pattern 19 and the 1- For example, the high-concentration arsenic ion whose dose pouring energy is 30keV(s) and is about [1x1016cm -] two is poured into the upper part of the semiconductor substrate 11. Then, by heat-treating to this semiconductor substrate 11, and activating arsenic ion Source field 32A of the N type in DMOSFET1, and drain contact field 32B of N type, And

1st source drain field 32C of the N type in MOSFET2 and 2nd source drain field 32D of N type are formed in a self-adjustment target to each sidewalls 31A, 31B, and 31C, respectively.
[0073] Next, as shown in drawing 8 (c), it deposits over the whole surface on the semiconductor substrate 11 using reduced pressure CVD by using as a layer insulation film the NSG film 21 whose thickness is about 800nm. Then, source field 32A [in / DMOSFET1 / to this NSG film 21 top], 1st insulated-gate electrode 14A, drain contact field 32B, and 1st source drain field 32C in MOSFET2, Form the resist pattern (not shown) which exposes a part of each upper surface of 3rd insulated-gate electrode 14C and 2nd source drain field 32D, and this resist pattern is used as a mask. By performing dry etching to the NSG film 21, a contact hole is formed, respectively. Then, after [for example,] depositing the metal membrane (not shown) which consists of aluminum etc. over the whole surface on the semiconductor substrate 11 using the sputtering method, By forming a predetermined resist pattern (not shown) on this metal membrane, and etching to this metal membrane by using this resist pattern as a mask 1st source drain wiring 22D in source wiring 22A in DMOSFET1, 1st gate wiring 22B, drain wiring 22C, and MOSFET2, 2nd gate wiring 22E, and the 2nd source drain wiring 22F are formed, respectively.
[0074] thus, 2nd insulated-gate electrode 14B of the dummy which is drain contact region specification-part material in the process which forms 1st insulated-gate electrode 14A of DMOSFET1 according to this operation gestalt -- forming -- this -- 2nd insulated-gate electrode 14B -- anti- -- 2nd sidewall 31B by the side of the 1st insulated-gate electrode -- using -- drain contact field 32B -- self -- it forms conformably Since it becomes unnecessary to expect the margin of the size of the resist film at the time of resist film formation conventionally unlike the drain contact field using the resist film and is hard coming to generate dispersion in the distance during source drain contact by this consequently, dispersion in the on resistance in DMOSFET1 is suppressed. Since drain contact region specification-part material is considered as the same composition as 1st insulated-gate electrode 14A and it moreover is not necessary to establish a new process, most costs which form drain contact region specification-part material can be disregarded.
[0075] Furthermore, in the process which forms each low concentration diffusion fields 18D and 18E in MOSFET2, since low resistance field 18C with larger high impurity concentration than the drain field 13 is prepared in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the semiconductor substrate 11, the effect that the on resistance of DMOSFET1 decreases arises, without adding a new process. In addition, needless to say, 2nd insulated-gate electrode 14B and low resistance field 18C which are this drain contact region specification-part material do not affect a property at all to MOSFET2.
[0076] Moreover, you may prepare the source drain extension member which has the same composition as 2nd insulated-gate electrode 14B of a dummy like the 1st modification of the 1st operation gestalt in the field between 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B in the principal plane of the semiconductor substrate 11.
[0077] (The 1st modification of the 2nd operation gestalt) It explains hereafter, referring to a drawing about the 1st modification of this operation gestalt.
[0078] Drawing 9 shows the cross-section composition of the semiconductor device concerning the 1st modification of the 2nd operation gestalt. In drawing 9 , explanation is omitted by giving the same sign to the same component as the component of drawing 6 . As shown in drawing 9 , wiring with 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B is electrically connected as a feature of this modification using the 1st gate wiring 22G so that 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B can control to this potential.
[0079] If voltage is impressed to the 1st gate wiring, in order that a carrier may focus on the field of the 2nd insulated-gate electrode 14B bottom in the upper part of the semiconductor substrate 11 by this, an on resistance decreases further. Moreover, the property of MOSFET2 is not affected at all, without the cost which manufacture of DMOSFET1 takes increasing, since a new process is not needed.
[0080] In addition, in the 1st and 2nd operation gestalten and each modifications, although each mold of the channel of DMOSFET1 and MOSFET2 was used as the N channel type, even if it is a P channel

type, it is clear to have the same effect.
[0081] moreover, the extension between source drains -- although the same configuration as an insulated-gate electrode and the same member were used for a member and drain contact position specification-part material, the field which touches the principal plane of not only this but a semiconductor substrate is an insulator, and a configuration will not be asked if it is the range from which the relation between pressure-proofing and an on resistance becomes good
[0082] Moreover, 1st insulated-gate electrode 14A and 2nd insulated-gate electrode 14B may be connected in the exterior of a DMOSFET1 formation field.
[0083]
[Effect of the Invention] According to the semiconductor device of this invention, since the position of the edge by the side of the source field in a drain contact field is regulated by the self-adjustment target according to the side by the side of the anti-source field of drain contact region specification-part material and dispersion in the distance during source drain contact is suppressed, dispersion in the on resistance specified in the distance during source drain contact decreases.
[0084] The semiconductor device of this invention is formed in the field between the insulated-gate electrodes and drain contact region specification-part material in the upper part of a semiconductor substrate. If the impurity of the 1st conductivity type is further equipped with the low resistance field where it comes to dope the high impurity concentration smaller [it is larger than a drain field, and] than a source field or a drain contact field Since resistance of the field between the insulated-gate electrodes and drain contact region specification-part material in a semiconductor substrate becomes small, an on resistance decreases and a property improves further.
[0085] In the semiconductor device of this invention, drain contact region specification-part material is certainly formed as an insulated-gate electrode is the 1st insulated-gate electrode and it is the 2nd insulated-gate electrode in which it insulated with the semiconductor substrate and drain contact region specification-part material was formed.
[0086] In the semiconductor device of this invention, if the 1st insulated-gate electrode and the 2nd insulated-gate electrode are connected electrically, since the resistance during the source drain contact under the 2nd insulated-gate electrode in a semiconductor substrate will become small, an on resistance decreases further.
[0087] The semiconductor device of this invention sets an interval to the field between the insulated-gate electrodes and drain contact region specification-part material on a semiconductor substrate, respectively, and is formed in it. The source drain extension member which the portion which touches a semiconductor substrate at least becomes from an insulator, It is formed in the field between the insulated-gate electrode in a semiconductor substrate, and a source drain extension member, and the field between a source drain extension member and drain contact region specification-part material, respectively. If the impurity of the 1st conductivity type is further equipped with the low resistance field where it comes to dope the high impurity concentration smaller [it is larger than a drain field, and] than a source field or a drain contact field Since a source drain extension member and drain contact region specification-part material are formed in the field between a source field and a drain contact field and between source drain contacts is extended the insulated-gate electrode in a semiconductor substrate while pressure-proofing improves, and extension, since the low resistance field where high impurity concentration is larger than a drain field is formed in the field between a member and position specification-part material Since resistance of the field between the insulated-gate electrodes and drain contact region specification-part material in a semiconductor substrate becomes small, the increase in an on resistance is suppressed.
[0088] In the semiconductor device of this invention, drain contact region specification-part material and a source drain extension member are certainly formed as an insulated-gate electrode is the 1st insulated-gate electrode, and it is the 2nd insulated-gate electrode in which it insulated with the semiconductor substrate and drain contact region specification-part material was formed and is the 3rd insulated-gate electrode which the source drain extension member was insulated with the semiconductor substrate, and was formed.

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[0089] In the semiconductor device of this invention, if the 1st insulated-gate electrode, the 2nd insulated-gate electrode, and the 3rd insulated-gate electrode are connected electrically, since the resistance during the source drain contact under the 2nd and 3rd insulated-gate electrodes in a semiconductor substrate will become small, an on resistance decreases further.
[0090] The source side impurity diffusion field which the semiconductor device of this invention is formed in the field between the soffit section sides of a source field the upper-limit section side of the body field in a semiconductor substrate, and has the same high-impurity-concentration profile as a low resistance field, If it was formed in the field between the soffit section sides of the drain field in a semiconductor substrate, and a drain contact field and has further the low resistance field and the drain contact side impurity diffusion field which has the same high-impurity-concentration profile Since electric field are eased in the interface of a source field and a body field, and the interface of a drain contact field and a drain field, pressure-proofing improves further.
[0091] In the semiconductor device of this invention in the both-sides side of the direction of gate length of an insulated-gate electrode and drain contact region specification-part material The side attachment wall which consists of an insulator layer, respectively sticks, is formed, and the position of the edge by the side of the drain contact field in a source field While being regulated by the self-adjustment target by the side attachment wall by the side of the anti-drain contact field of an insulated-gate electrode, the position of the edge by the side of the source field in a drain contact field If regulated by the self-adjustment target by the side attachment wall by the side of the anti-source field of drain contact region specification-part material, since a source field and a drain contact field will serve as LDD structure, pressure-proofing improves further.
[0092] Since according to the manufacture method of the 1st semiconductor device of this invention the position of the edge by the side of the source field in a drain contact field is regulated by the side by the side of the anti-source field of the 2nd insulated-gate electrode and dispersion in the distance during source drain contact can be suppressed, dispersion in an on resistance can be decreased.
[0093] Since according to the manufacture method of the 2nd semiconductor device of this invention the position of the edge by the side of the source field in a drain contact field is regulated by the 2nd side attachment wall by the side of the anti-source field of the 2nd insulated-gate electrode and dispersion in the distance during source drain contact can be suppressed, dispersion in an on resistance can be decreased.
[0094] Furthermore, since a source field and a drain contact field have LDD structure, respectively, pressure-proofing improves further.
[0095] The 1st of this invention or the manufacture method of the 2nd semiconductor device to the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode in a semiconductor substrate When high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field If it has further the impurity diffusion field formation process which forms an impurity diffusion field in the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode Since the impurity diffusion field formed between the insulated-gate electrode of 1 and the 2nd insulated-gate electrode has high impurity concentration larger than a drain field and resistance becomes small rather than a drain field, an on resistance can be reduced.
[0096] The field between the upper-limit sections of a body field and the soffit sections of a source field, [in / a semiconductor substrate / on the 1st of this invention, or the manufacture method of the 2nd semiconductor device, and / in an impurity diffusion field formation process] When high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field to the field between the soffit sections of a drain field and a drain contact field If the process which forms an impurity diffusion field in each field between the upper-limit section of a body field and the soffit section of a source field and between the soffit sections of a drain field and a drain contact field, respectively is included Since electric field are eased in the interface of a source field and a body field, and the interface of a drain contact field and a drain field, pressure-proofing improves further.

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[0097] DMOSFET by which dispersion in an on resistance was suppressed can be manufactured without [in order according to the manufacture method of the 3rd semiconductor device of this invention to acquire the effect of the manufacture method of the 1st semiconductor device upwards and to form the 1st insulated-gate electrode for DMOSFET, the 2nd insulated-gate electrode of a dummy, and the 3rd insulated-gate electrode for MOSFET at the process of 1, without the cost which manufacture of a semiconductor device takes increases, and] affecting the electrical property of MOSFET
[0098] DMOSFET by which dispersion in an on resistance was suppressed can be manufactured without [in order according to the manufacture method of the 4th semiconductor device of this invention to acquire the effect of the manufacture method of the 3rd semiconductor device upwards and to form the 1st insulated-gate electrode for DMOSFET, the 2nd insulated-gate electrode of a dummy, and the 3rd insulated-gate electrode for MOSFET at the process of 1 without the cost which manufacture of a semiconductor device takes increases, and] affecting the electrical property of MOSFET Moreover, since a source field and a drain contact field have LDD structure, respectively, pressure-proofing improves further.
[0099] The 3rd of this invention or the manufacture method of the 4th semiconductor device to the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode in a semiconductor substrate When high impurity concentration dopes the impurity of the 1st larger and conductivity type smaller than a source field or a drain contact field than a drain field If it has further the impurity diffusion field formation process which forms an impurity diffusion field in the field between the 1st insulated-gate electrode and the 2nd insulated-gate electrode Since the impurity diffusion field formed between the insulated-gate electrode of 1 and the 2nd insulated-gate electrode has high impurity concentration larger than a drain field and resistance becomes small rather than a drain field, an on resistance can be reduced.
[0100] In the 3rd of this invention, or the manufacture method of the 4th semiconductor device an impurity diffusion field formation process The process which forms an impurity diffusion field in each field between the upper-limit section of a body field, and the soffit section of a source field, and between the soffit sections of a drain field and a drain contact field, respectively, Since the process formed in the field by the side of the soffit section of the 1st source drain field and the field by the side of the soffit section of the 2nd source drain field, respectively is included, the LDD structure of DMOSFET and MOSFET can be certainly formed at the process of 1.
[0101] If the manufacture method of the 1-4th semiconductor devices of this invention is further equipped with the process which connects electrically the 1st insulated-gate electrode and the 2nd insulated-gate electrode, since the resistance during the source drain contact under the 2nd insulated-gate electrode in a semiconductor substrate will become small, an on resistance decreases further.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the composition cross section showing the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 2] It is the order cross section of a process showing the manufacture method of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 3] It is the order cross section of a process showing the manufacture method of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 4] It is the composition cross section showing the semiconductor device concerning the 1st modification of the 1st operation gestalt of this invention.
[Drawing 5] It is the composition cross section showing the semiconductor device concerning the 2nd modification of the 1st operation gestalt of this invention.
[Drawing 6] It is the composition cross section showing the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 7] It is the order cross section of a process showing the manufacture method of the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 8] It is the order cross section of a process showing the manufacture method of the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 9] It is the composition cross section showing the semiconductor device concerning the 1st modification of the 2nd operation gestalt of this invention.
[Drawing 10] It is the order cross section of a process showing the manufacture method of the conventional DMOSFET.
[Description of Notations]
1 DMOSFET
2 MOSFET
11 Semiconductor Substrate
12 1st Resist Pattern
13 Drain Field
14A The 1st insulated-gate electrode
14B The 2nd insulated-gate electrode (drain contact region specification-part material)
14C The 3rd insulated-gate electrode
14D The 4th insulated-gate electrode (source drain extension member)
15 2nd Resist Pattern
16 Body Field
17 3rd Resist Pattern
18A Source side impurity diffusion field
18B Drain contact side impurity diffusion field
18C Low resistance field
18D The 1st low concentration diffusion field

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18E The 2nd low concentration diffusion field
19 4th Resist Pattern
20A Source field
20B Drain contact field
20C The 1st source drain field
20D The 2nd source drain field
21 NSG Film
22A Source wiring
22B 1st gate wiring
22C Drain wiring
22D 1st source drain wiring
22E 2nd gate wiring
22F 2nd source drain wiring
22G 1st gate wiring
24 Gate Oxide Film
25 Polycrystal Silicon Film
31A The 1st sidewall
31B The 2nd sidewall
31C The 3rd sidewall
32A Source field
32B Drain contact field
32C The 1st source drain field
32D The 2nd source drain field

[Translation done.]

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* NOTICES *

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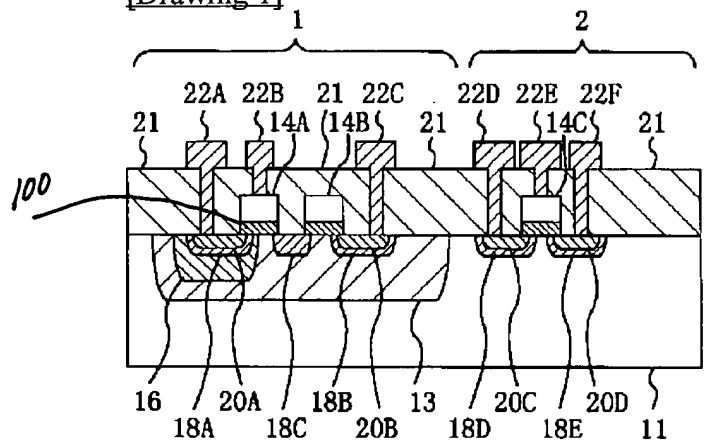
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



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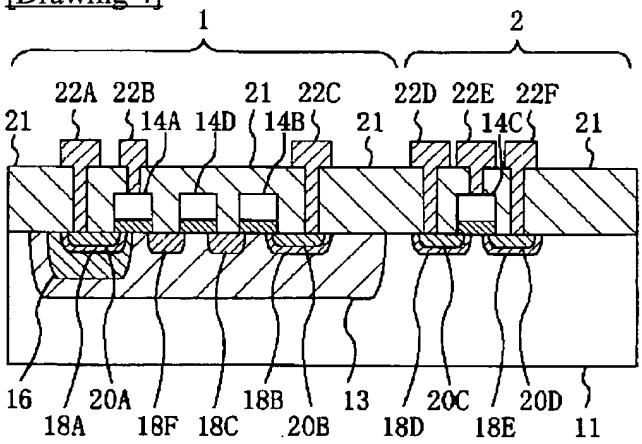

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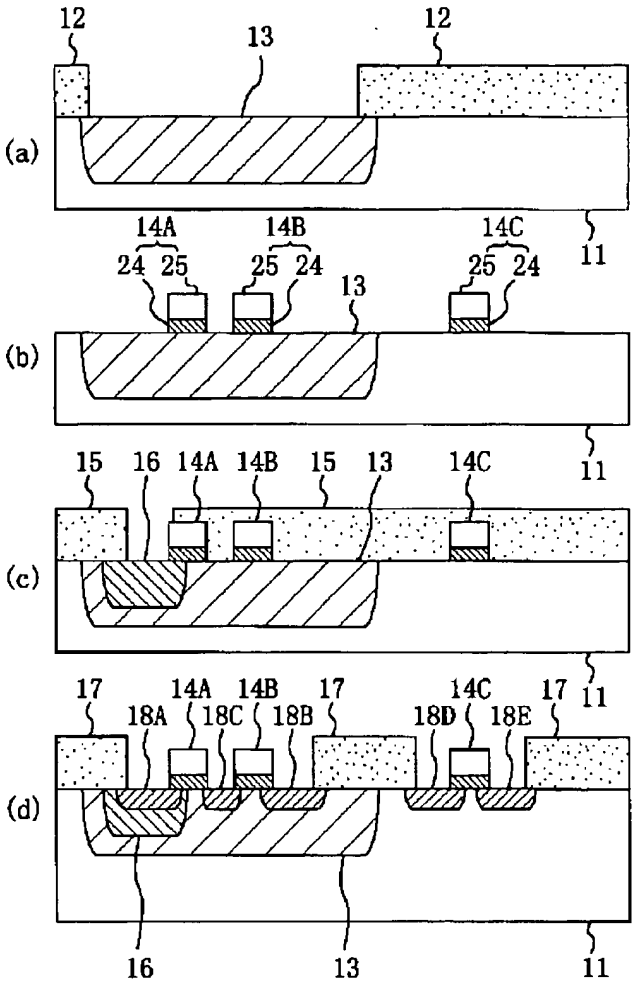

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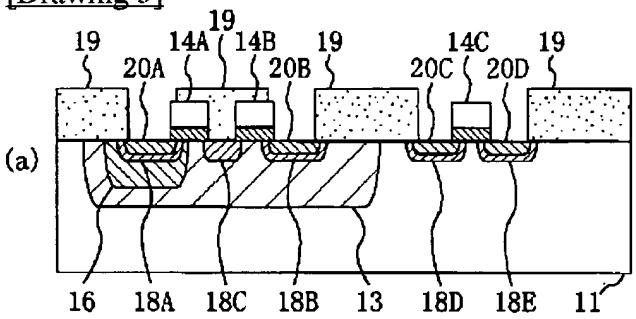

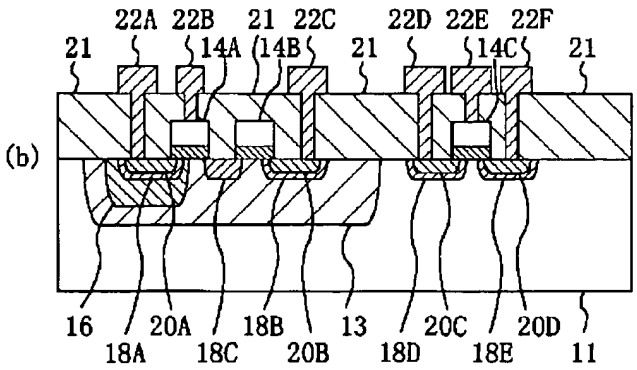

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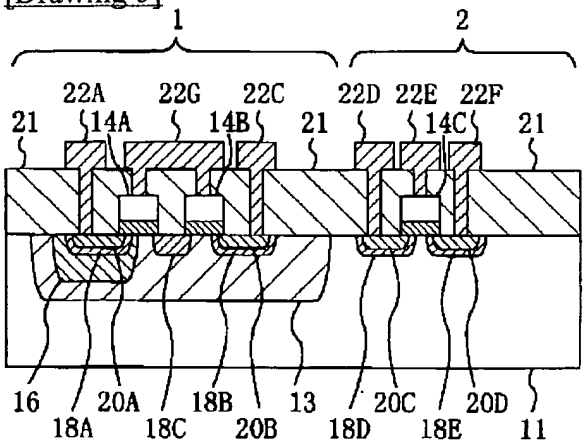
[Drawing 5]



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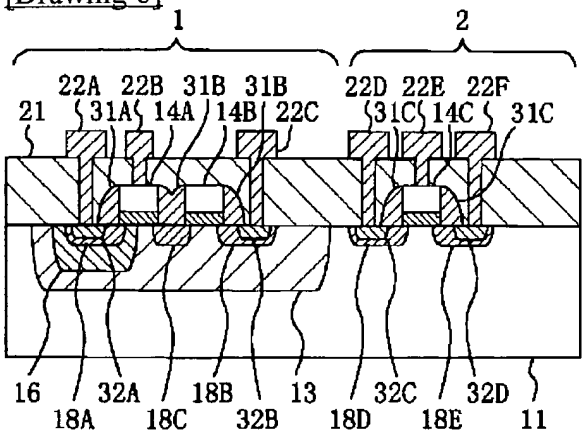

[Drawing 7]

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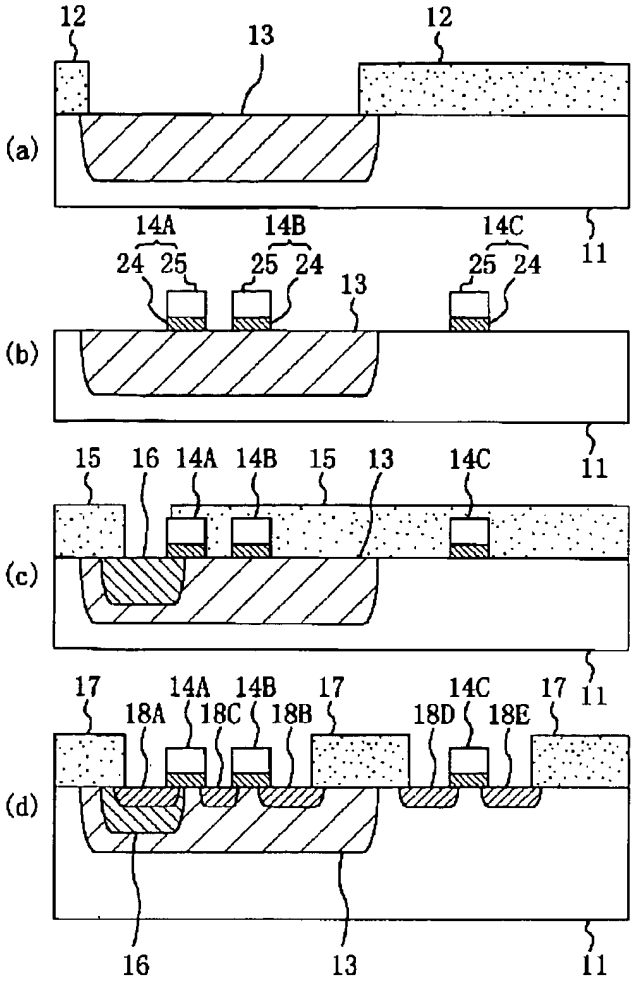

[Drawing 8]

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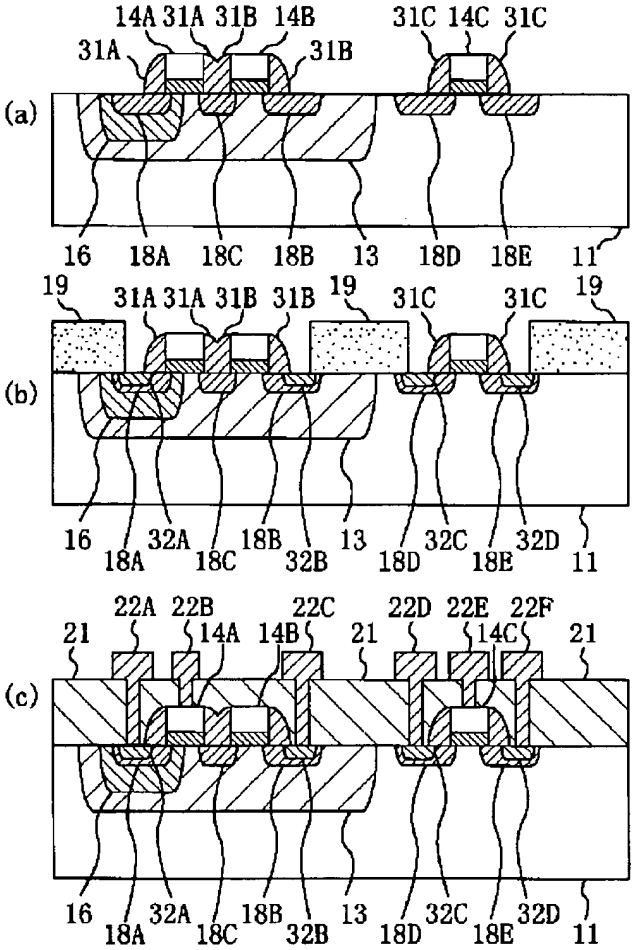

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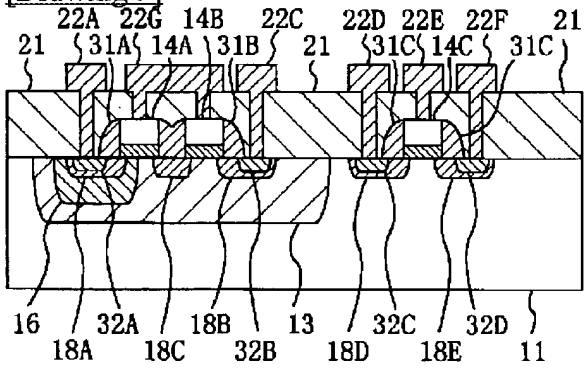

[Drawing 10]

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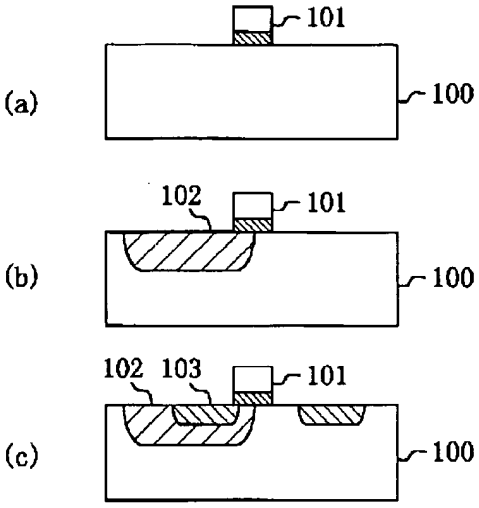

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SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-031816 [JP 11031816 A]
PUBLISHED: February 02, 1999 (19990202)
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APPL. NO.: 09-188058 [JP 97188058]
FILED: July 14, 1997 (19970714)
INTL CLASS: H01L-029/78; H01L-021/8238; H01L-027/092

ABSTRACT

PROBLEM TO BE SOLVED: To decrease variations in on the resistances of DMOSFETs in a semiconductor device having DMOSFETs.

SOLUTION: A DMOSFET 1 and a MOSFET 2 are formed on a semiconductor substrate 11 of P-type silicon. A first insulating gate electrode 14A and a dummy second insulating gate electrode 14B as a member for controlling the position of a drain contact region are formed at an established interval on an N-type drain region 13 of the DMOSFET 1. In the drain region 13, a P-type body region 16 is formed in self-alignment with respect to the first insulating gate electrode 14A in the region opposing second insulating region, and an N-type drain contact region 20B is formed in self-alignment with the second insulating gate electrode 14B in the region opposing first insulating region.